Integrated Technical Education Cluster
At AlAmeeria

J-601-1448
Electronic Principals

Lecture #4
BJT AC Analysis

Instructor:
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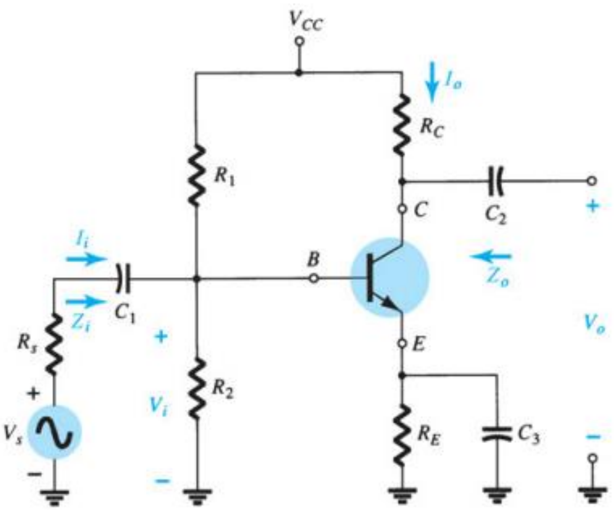
Agenda

- BJT transistor Modeling
- The r_e Transistor Model (small signal analysis)
- Effect of R_L and R_s & determining the Current Gain
- Two-Port Systems Approach
- Cascaded Systems
- The Hybrid Equivalent Model (Approximate & Complete)
- Troubleshooting and Practical Applications

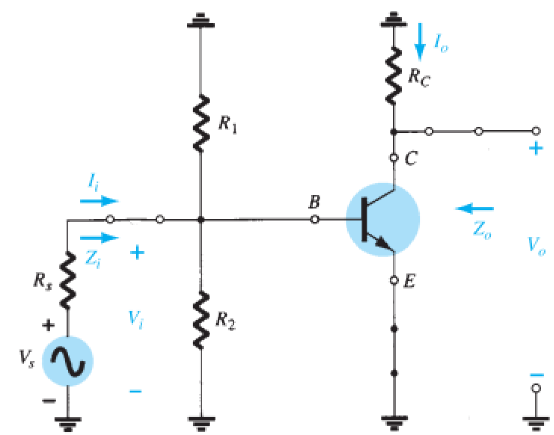
BJT TRANSISTOR MODELING

BJT Transistor Modeling

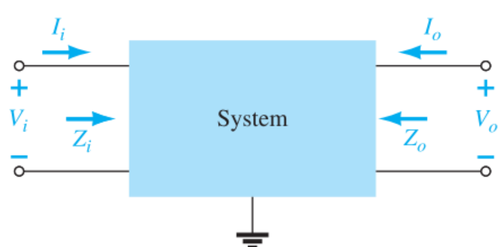
- A model is a combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.

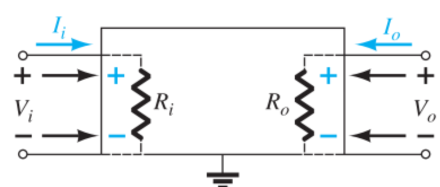


Ac analysis



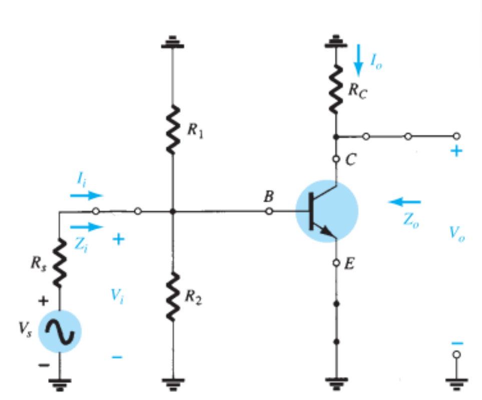
- Defining the important parameters of any system.

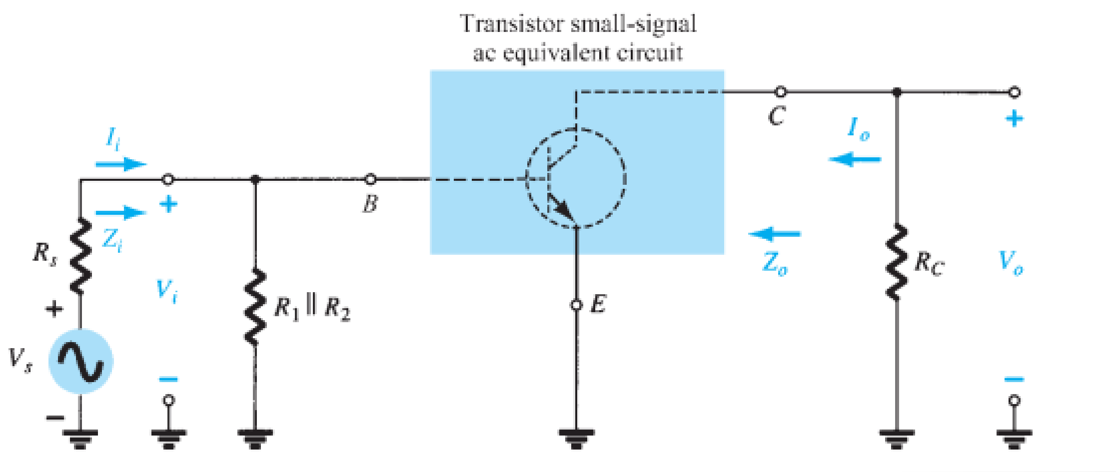




BJT Transistor Modeling

- the ac equivalent of a transistor network is obtained by:
  1. Setting all dc sources to zero and replacing them by a short-circuit equivalent
  2. Replacing all capacitors by a short-circuit equivalent
  3. Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2
  4. Redrawing the network in a more convenient and logical form





- Common Emitter Configuration
- Common Base Configuration
- Common Collector Configuration
- r_e Model in Different Bias Circuits

THE r_e TRANSISTOR MODEL

The r_e Transistor Model (CE)

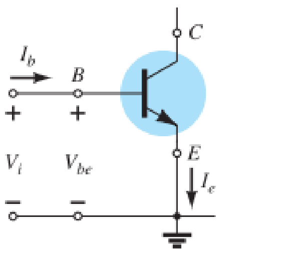


FIG. 5.8
Finding the input equivalent circuit for a BJT transistor.

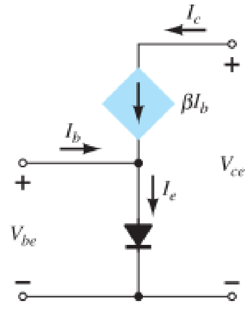


FIG. 5.12
BJT equivalent circuit.

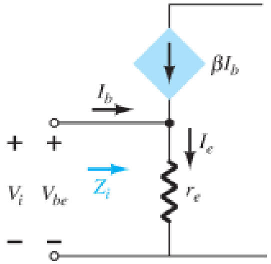


FIG. 5.13
Defining the level of Z_i.

$$Z_i = \frac{V_i}{I_b} = \frac{V_{be}}{I_b}$$

$$V_{be} = I_e r_e = (I_c + I_b) r_e = (\beta I_b + I_b) r_e$$

$$= (\beta + 1) I_b r_e$$

$$Z_i = \frac{V_{be}}{I_b} = \frac{(\beta + 1) I_b r_e}{I_b}$$

$$\boxed{Z_i = (\beta + 1) r_e \cong \beta r_e}$$

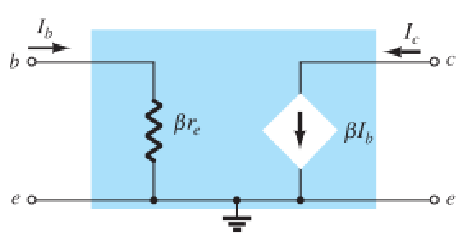


FIG. 5.14
Improved BJT equivalent circuit.

Early Voltage

$$\boxed{r_o = \frac{\Delta V}{\Delta I} = \frac{V_A + V_{CE_Q}}{I_{C_Q}}}$$

$$\boxed{r_o \cong \frac{V_A}{I_{C_Q}}}$$

$$\text{Slope} = \frac{\Delta y}{\Delta x} = \frac{\Delta I_C}{\Delta V_{CE}} = \frac{1}{r_o}$$

$$\boxed{r_o = \frac{\Delta V_{CE}}{\Delta I_C}}$$

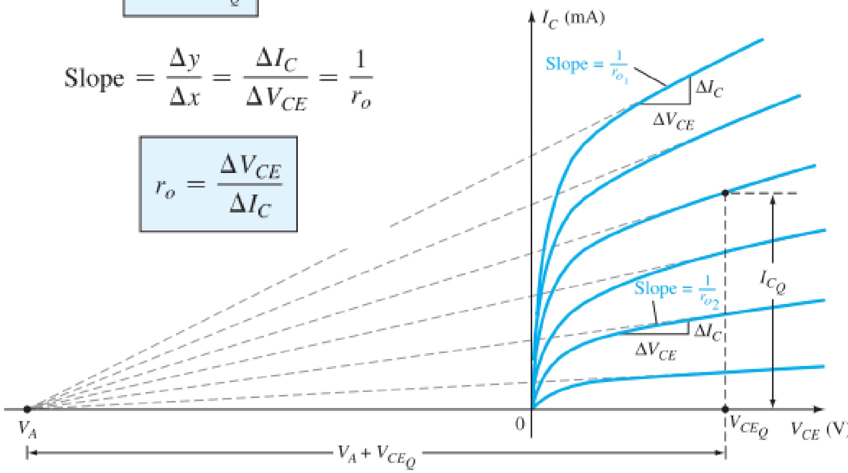


FIG. 5.15
Defining the Early voltage and the output impedance of a transistor.

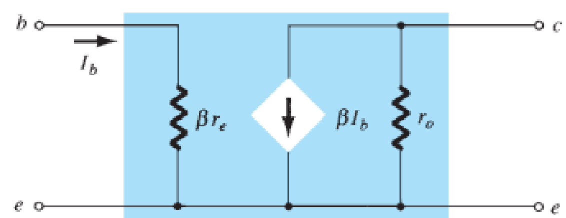


FIG. 5.16
r_e model for the common-emitter transistor configuration including effects of r_o.

The r_e Transistor Model (CB)

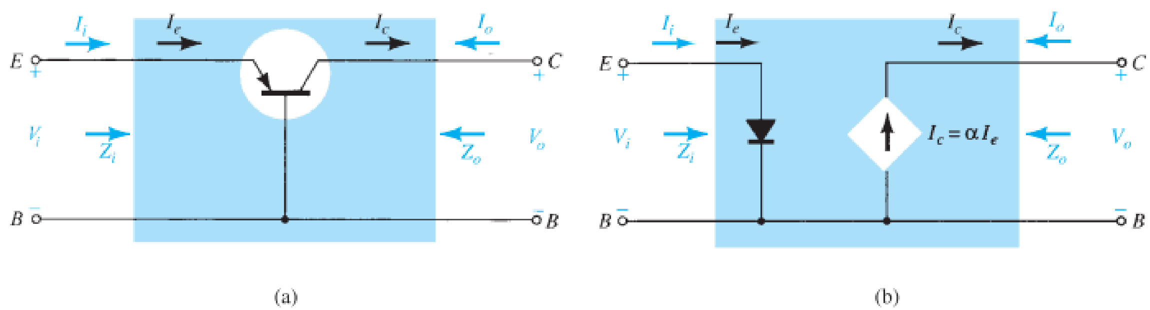


FIG. 5.17
(a) Common-base BJT transistor; (b) equivalent circuit for configuration of (a).

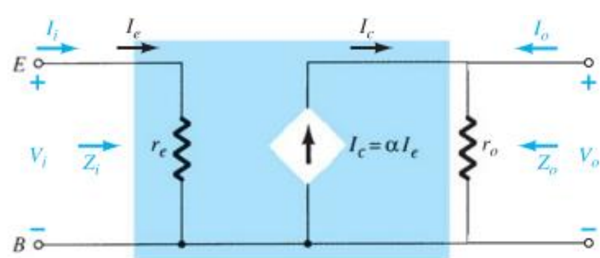


FIG. 5.18
Common base r_e equivalent circuit.

The r_e Transistor Model (CC)

- For the common-collector configuration, the model defined for the common-emitter configuration of is normally applied rather than defining a model for the common-collector configuration.

npn versus pnp

- The dc analysis of *npn* and *pnp* configurations is quite different in the sense that the currents will have opposite directions and the voltages opposite polarities.
- However, for an ac analysis where the signal will progress between positive and negative values, the ac equivalent circuit will be the same.

C.E. Fixed Bias Configuration

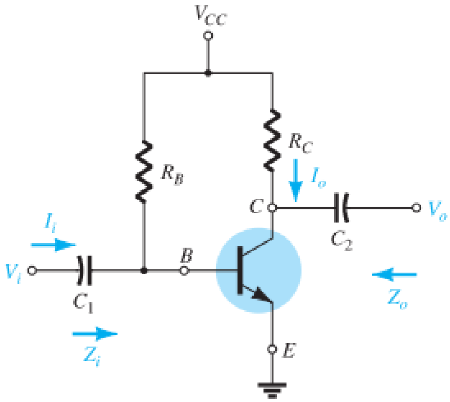


FIG. 5.20
Common-emitter fixed-bias configuration.

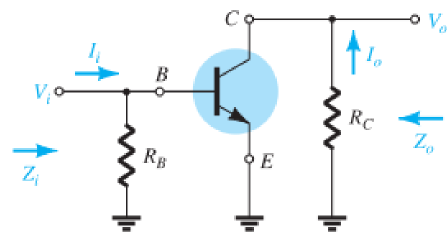


FIG. 5.21
Network of Fig. 5.20 following the removal of the effects of V_{CC}, C_1, and C_2.

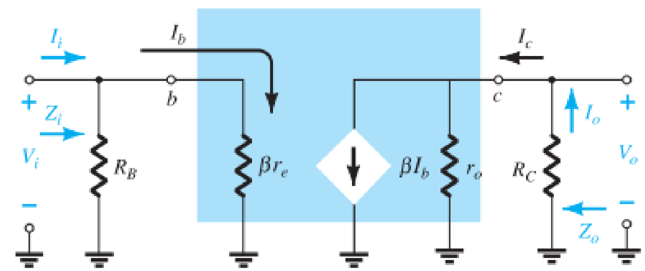


FIG. 5.22
Substituting the r_e model into the network of Fig. 5.21.

Phase Relationship

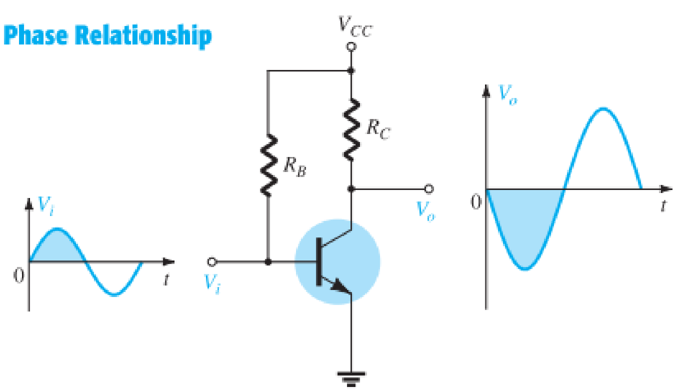


FIG. 5.24
Demonstrating the 180° phase shift between input and output waveforms.

$$\boxed{Z_i = R_B \| \beta r_e} \quad \text{ohms}$$

$$\boxed{Z_i \cong \beta r_e} \quad {}_{R_B \geq 10\beta r_e} \quad \text{ohms}$$

$$\boxed{Z_o = R_C \| r_o} \quad \text{ohms}$$

$$\boxed{Z_o \cong R_C} \quad {}_{r_o \geq 10R_C}$$

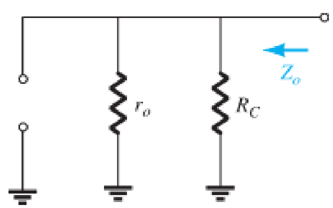


FIG. 5.23
Determining Z_o for the network of Fig. 5.22.

$$V_o = -\beta I_b (R_C \| r_o)$$

$$I_b = \frac{V_i}{\beta r_e}$$

$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{(R_C \| r_o)}{r_e}}$$

$$\boxed{A_v = -\frac{R_C}{r_e}} \quad {}_{r_o \geq 10R_C}$$

Voltage-Divider Bias

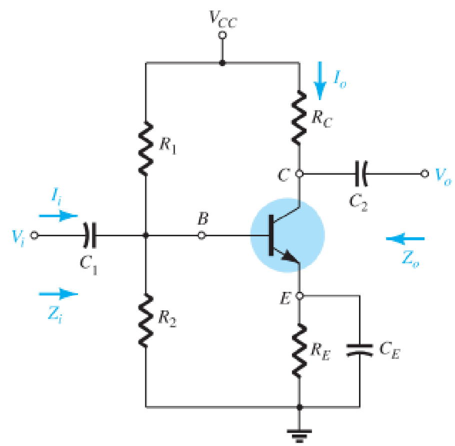


FIG. 5.26
Voltage-divider bias configuration.

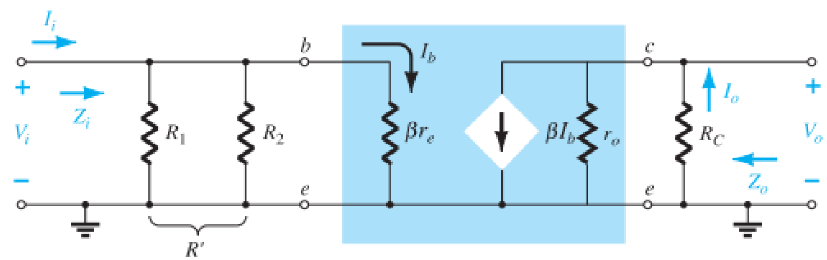


FIG. 5.27
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.26.

$$\boxed{R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}}$$

$$\boxed{Z_i = R' \| \beta r_e}$$

$$\boxed{Z_o = R_C \| r_o}$$

$$\boxed{Z_o \cong R_C} \quad {}_{r_o \geq 10R_C}$$

$$V_o = -(\beta I_b)(R_C \| r_o)$$

$$I_b = \frac{V_i}{\beta r_e}$$

$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{-R_C \| r_o}{r_e}}$$

180° phase shift

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e}} \quad {}_{r_o \geq 10R_C}$$

EFFECT OF R_L AND R_S (SYSTEM APPROACH)

Effect of R_L and R_s

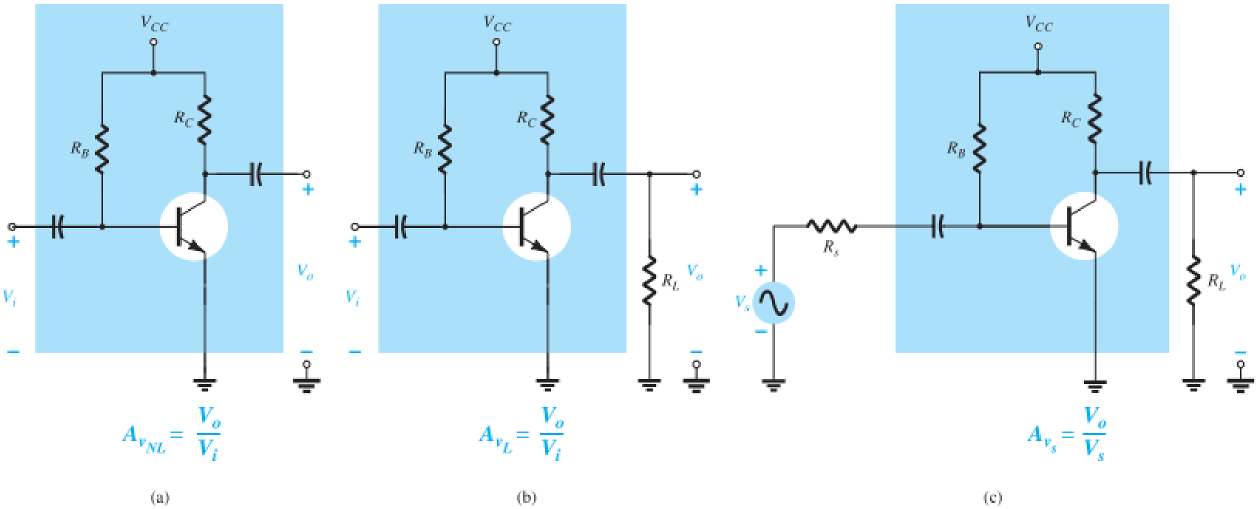


FIG. 5.54
Amplifier configurations: (a) unloaded; (b) loaded; (c) loaded with a source resistance.

$$\boxed{A_{v_{NL}} = \frac{V_o}{V_i}}$$

$$\boxed{A_{v_L} = \frac{V_o}{V_i}} \quad \text{with } R_L$$

$$\boxed{A_{v_s} = \frac{V_o}{V_s}} \quad \text{with } R_L \text{ and } R_s$$

- The loaded voltage gain of an amplifier is always less than the no-load gain.
- The gain obtained with a source resistance in place will always be less than that obtained under loaded or unloaded conditions due to the drop in applied voltage across the source resistance.
- For the same configuration $A_{vNL} > A_{vL} > A_{vs}$.
- For a particular design, the larger the level of R L , the greater is the level of ac gain.
- For a particular amplifier, the smaller the internal resistance of the signal source, the greater is the overall gain.
- For any network that have coupling capacitors, the source and load resistance do not affect the dc biasing levels.

Effect of R_L and R_s ..

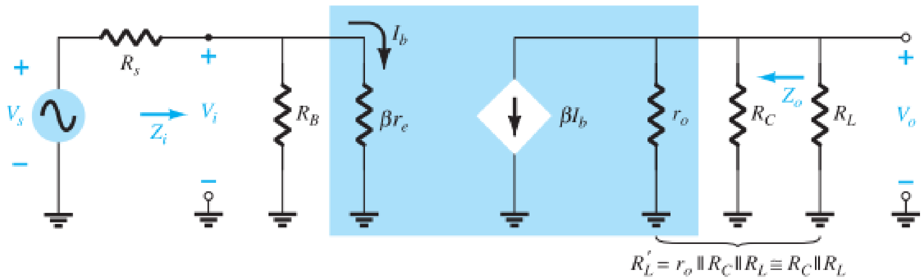


FIG. 5.55
The ac equivalent network for the network of Fig. 5.54c.

$$R'_L = r_o \| R_C \| R_L \cong R_C \| R_L$$

$$V_o = -\beta I_b R'_L = -\beta I_b (R_C \| R_L)$$

$$I_b = \frac{V_i}{\beta r_e}$$

$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| R_L)$$

$$\boxed{A_{v_L} = \frac{V_o}{V_i} = -\frac{R_C \| R_L}{r_e}}$$

$$V_i = \frac{Z_i V_s}{Z_i + R_s}$$

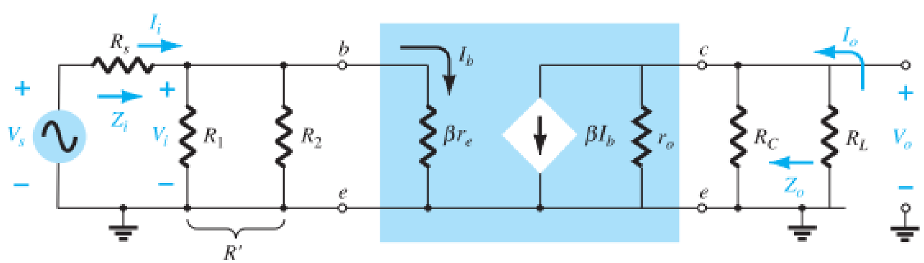
$$\frac{V_i}{V_s} = \frac{Z_i}{Z_i + R_s}$$

$$A_{v_S} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s} = A_{v_L} \frac{Z_i}{Z_i + R_s}$$

$$\boxed{A_{v_S} = \frac{Z_i}{Z_i + R_s} A_{v_L}}$$

$$\boxed{Z_i = R_B \| \beta r_e} \qquad \boxed{Z_o = R_C \| r_o}$$

Voltage-divider ct.



$$\boxed{A_{v_L} = \frac{V_o}{V_i} = -\frac{R_C \| R_L}{r_e}}$$

$$\boxed{Z_i = R_1 \| R_2 \| \beta r_e}$$

$$\boxed{Z_o = R_C \| r_o}$$

$$\boxed{A_{v_L} = \frac{V_o}{V_i} = \frac{R_E \| R_L}{R_E \| R_L + r_e}}$$

DETERMINING THE CURRENT GAIN

Determining the Current gain

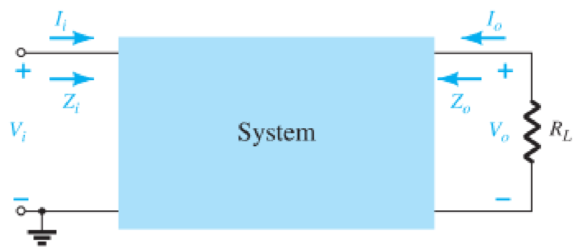


FIG. 5.60
Determining the current gain using the voltage gain.

- For each transistor configuration, the current gain can be determined directly from the voltage gain, the defined load, and the input impedance.

$$A_i = \frac{I_o}{I_i}$$

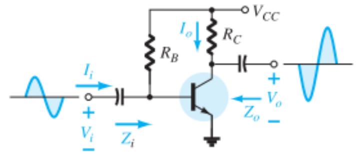
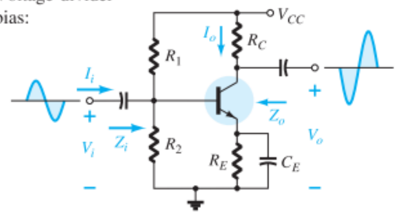
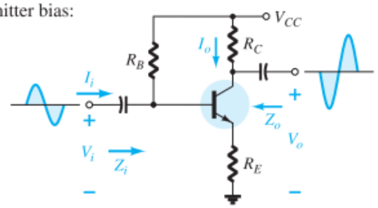
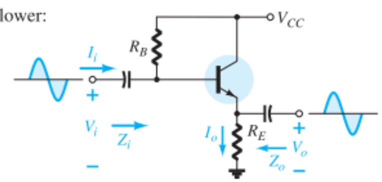
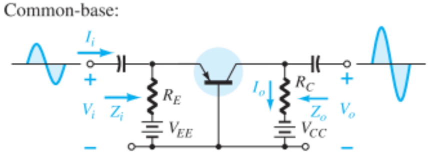
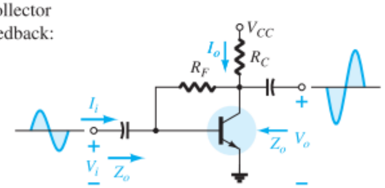
$$I_i = \frac{V_i}{Z_i} \quad \text{and} \quad I_o = -\frac{V_o}{R_L}$$

$$A_{i_L} = \frac{I_o}{I_i} = \frac{-\dfrac{V_o}{R_L}}{\dfrac{V_i}{Z_i}} = -\frac{V_o}{V_i} \cdot \frac{Z_i}{R_L}$$

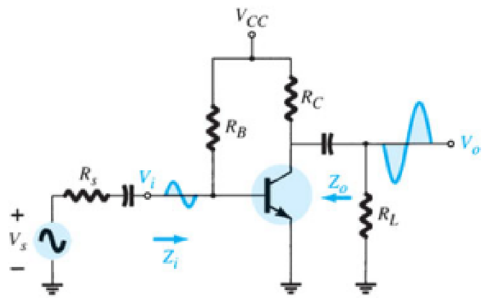
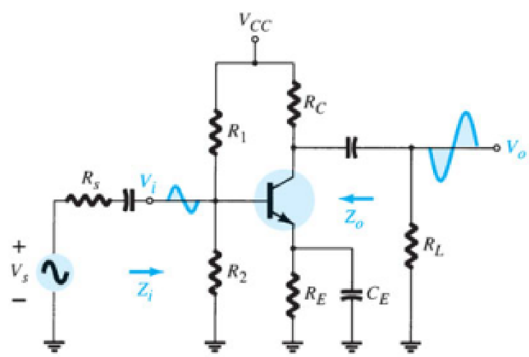
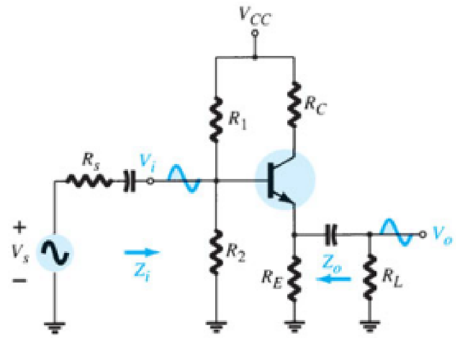
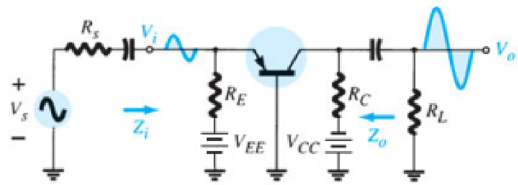
$$\boxed{A_{i_L} = -A_{v_L}\frac{Z_i}{R_L}}$$

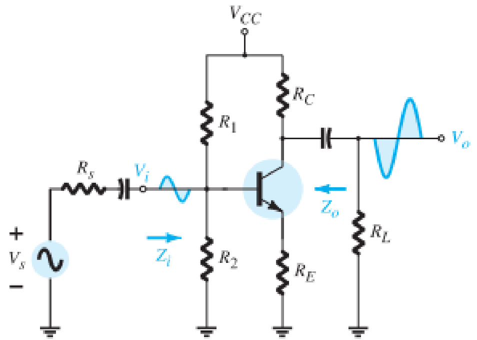
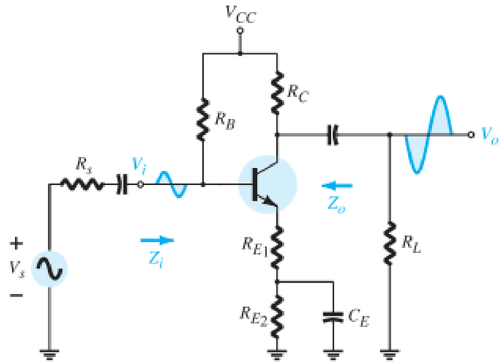
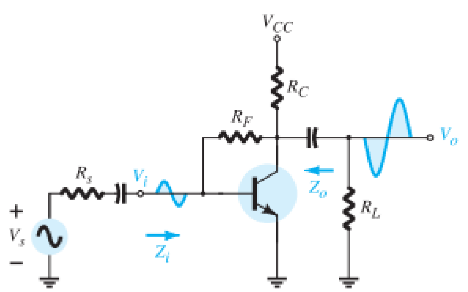
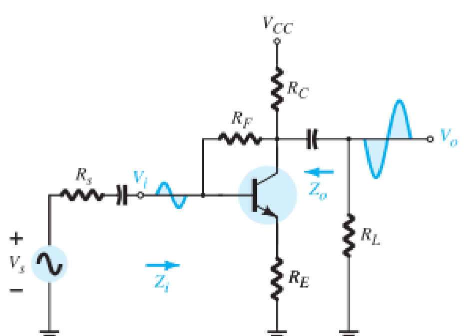
SUMMARY TABLE

Unloaded BJT Transistor Amplifiers

Configuration	Z_i	Z_o	A_v	A_i
Fixed-bias: 	Medium (1 kΩ) $= \boxed{R_B \| \beta r_e}$ $\cong \boxed{\beta r_e}$ $(R_B \geq 10\beta r_e)$	Medium (2 kΩ) $= \boxed{R_C \| r_o}$ $\cong \boxed{R_C}$ $(r_o \geq 10R_C)$	High (−200) $= \boxed{-\frac{(R_C \| r_o)}{r_e}}$ $\cong \boxed{-\frac{R_C}{r_e}}$ $(r_o \geq 10R_C)$	High (100) $= \boxed{\frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}}$ $\cong \boxed{\beta}$ $(r_o \geq 10R_C,$ $R_B \geq 10\beta r_e)$
Voltage-divider bias: 	Medium (1 kΩ) $= \boxed{R_1 \| R_2 \| \beta r_e}$	Medium (2 kΩ) $= \boxed{R_C \| r_o}$ $\cong \boxed{R_C}$ $(r_o \geq 10R_C)$	High (−200) $= \boxed{-\frac{R_C \| r_o}{r_e}}$ $\cong \boxed{-\frac{R_C}{r_e}}$ $(r_o \geq 10R_C)$	High (50) $= \boxed{\frac{\beta(R_1 \| R_2) r_o}{(r_o + R_C)(R_1 \| R_2 + \beta r_e)}}$ $\cong \boxed{\frac{\beta(R_1 \| R_2)}{R_1 \| R_2 + \beta r_e}}$ $(r_o \geq 10R_C)$
Unbypassed emitter bias: 	High (100 kΩ) $= \boxed{R_B \| Z_b}$ $Z_b \cong \beta(r_e + R_E)$ $\cong \boxed{R_B \| \beta R_E}$ $(R_E \gg r_e)$	Medium (2 kΩ) $= \boxed{R_C}$ (any level of r_o)	Low (−5) $= \boxed{-\frac{R_C}{r_e + R_E}}$ $\cong \boxed{-\frac{R_C}{R_E}}$ $(R_E \gg r_e)$	High (50) $\cong \boxed{-\frac{\beta R_B}{R_B + Z_b}}$
Emitter-follower: 	High (100 kΩ) $= \boxed{R_B \| Z_b}$ $Z_b \cong \beta(r_e + R_E)$ $\cong \boxed{R_B \| \beta R_E}$ $(R_E \gg r_e)$	Low (20 Ω) $= \boxed{R_E \| r_e}$ $\cong \boxed{r_e}$ $(R_E \gg r_e)$	Low (≅1) $= \boxed{\frac{R_E}{R_E + r_e}}$ $\cong \boxed{1}$	High (−50) $\cong \boxed{-\frac{\beta R_B}{R_B + Z_b}}$
Common-base: 	Low (20 Ω) $= \boxed{R_E \| r_e}$ $\cong \boxed{r_e}$ $(R_E \gg r_e)$	Medium (2 kΩ) $= \boxed{R_C}$	High (200) $\cong \boxed{\frac{R_C}{r_e}}$	Low (−1) $\cong \boxed{-1}$
Collector feedback: 	Medium (1 kΩ) $= \boxed{\frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}}}$ $(r_o \geq 10R_C)$	Medium (2 kΩ) $\cong \boxed{R_C \| R_F}$ $(r_o \geq 10R_C)$	High (−200) $\cong \boxed{-\frac{R_C}{r_e}}$ $(r_o \geq 10R_C)$ $(R_F \gg R_C)$	High (50) $= \boxed{\frac{\beta R_F}{R_F + \beta R_C}}$ $\cong \boxed{\frac{R_F}{R_C}}$

BJT Transistor Amplifiers Including the Effect of R_s and R_L

Configuration	$A_{v_L} = V_o/V_i$	Z_i	Z_o
	$\dfrac{-(R_L \parallel R_C)}{r_e}$	$R_B \parallel \beta r_e$	R_C
	Including r_o: $-\dfrac{(R_L \parallel R_C \parallel r_o)}{r_e}$	$R_B \parallel \beta r_e$	$R_C \parallel r_o$
	$\dfrac{-(R_L \parallel R_C)}{r_e}$	$R_1 \parallel R_2 \parallel \beta r_e$	R_C
	Including r_o: $\dfrac{-(R_L \parallel R_C \parallel r_o)}{r_e}$	$R_1 \parallel R_2 \parallel \beta r_e$	$R_C \parallel r_o$
	$\cong 1$	$R'_E = R_L \parallel R_E$ $R_1 \parallel R_2 \parallel \beta(r_e + R'_E)$	$R'_s = R_s \parallel R_1 \parallel R_2$ $R_E \parallel \left(\dfrac{R'_s}{\beta} + r_e\right)$
	Including r_o: $\cong 1$	$R_1 \parallel R_2 \parallel \beta(r_e + R'_E)$	$R_E \parallel \left(\dfrac{R'_s}{\beta} + r_e\right)$
	$\cong \dfrac{-(R_L \parallel R_C)}{r_e}$	$R_E \parallel r_e$	R_C
	Including r_o: $\cong \dfrac{-(R_L \parallel R_C \parallel r_o)}{r_e}$	$R_E \parallel r_e$	$R_C \parallel r_o$

	$\dfrac{-(R_L \Vert R_C)}{R_E}$	$R_1 \Vert R_2 \Vert \beta(r_e + R_E)$	R_C
	Including r_o: $\dfrac{-(R_L \Vert R_C)}{R_E}$	$R_1 \Vert R_2 \Vert \beta(r_e + R_e)$	$\cong R_C$
	$\dfrac{-(R_L \Vert R_C)}{R_{E_1}}$	$R_B \Vert \beta(r_e + R_{E_1})$	R_C
	Including r_o: $\dfrac{-(R_L \Vert R_C)}{R_{E_1}}$	$R_B \Vert \beta(r_e + R_E)$	$\cong R_C$
	$\dfrac{-(R_L \Vert R_C)}{r_e}$	$\beta r_e \Vert \dfrac{R_F}{\lvert A_v \rvert}$	R_C
	Including r_o: $\dfrac{-(R_L \Vert R_C \Vert r_o)}{r_e}$	$\beta r_e \Vert \dfrac{R_F}{\lvert A_v \rvert}$	$R_C \Vert R_F \Vert r_o$
	$\dfrac{-(R_L \Vert R_C)}{R_E}$	$\beta R_E \Vert \dfrac{R_F}{\lvert A_v \rvert}$	$\cong R_C \Vert R_F$
	Including r_o: $\cong \dfrac{-(R_L \Vert R_C)}{R_E}$	$\cong \beta R_E \Vert \dfrac{R_F}{\lvert A_v \rvert}$	$\cong R_C \Vert R_F$

TWO PORT SYSTEMS APPROACH

2-Port System

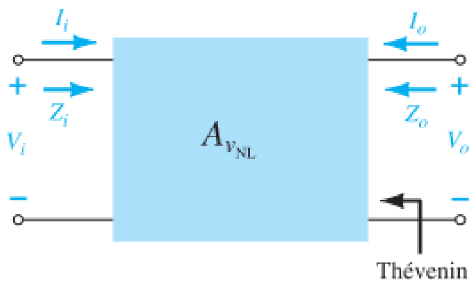
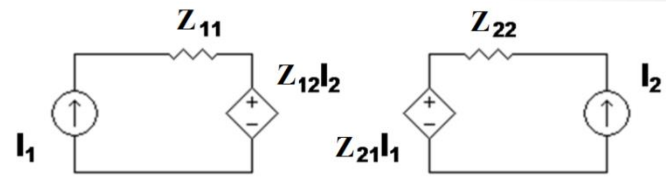


FIG. 5.61
Two-port system.

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$



where

$$z_{11} \stackrel{\text{def}}{=} \left.\frac{V_1}{I_1}\right|_{I_2=0} \qquad z_{12} \stackrel{\text{def}}{=} \left.\frac{V_1}{I_2}\right|_{I_1=0}$$

$$z_{21} \stackrel{\text{def}}{=} \left.\frac{V_2}{I_1}\right|_{I_2=0} \qquad z_{22} \stackrel{\text{def}}{=} \left.\frac{V_2}{I_2}\right|_{I_1=0}$$

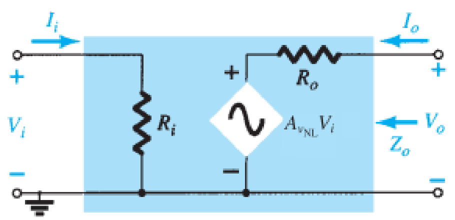


FIG. 5.62
Substituting the internal elements for the two-port system of Fig. 5.61.

$$\boxed{V_o = A_{v_{NL}} V_i}$$

$$\boxed{Z_o = R_o} \qquad \boxed{Z_i = R_i}$$

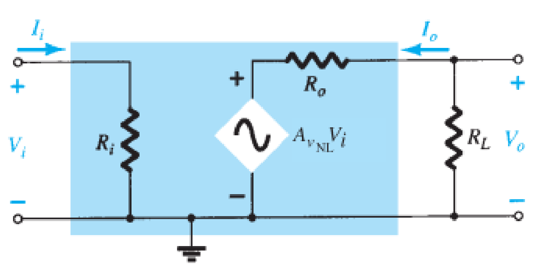


FIG. 5.63
Applying a load to the two-port system of Fig. 5.62.

$$V_o = \frac{R_L A_{v_{NL}} V_i}{R_L + R_o}$$

$$\boxed{A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} A_{v_{NL}}}$$

$$A_{i_L} = \frac{I_o}{I_i} = \frac{-V_o/R_L}{V_i/Z_i} = -\frac{V_o}{V_i}\frac{Z_i}{R_L}$$

$$\boxed{A_{i_L} = -A_{v_L}\frac{Z_i}{R_L}}$$

2-Port System..

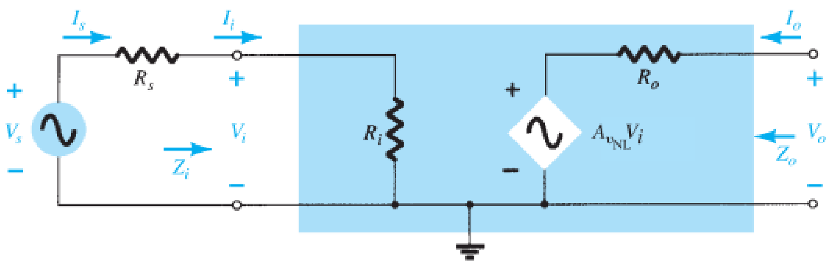


FIG. 5.64
Including the effects of the source resistance R_s.

$$\boxed{V_i = \frac{R_i V_s}{R_i + R_s}}$$

$$V_o = A_{v_{NL}} V_i$$

$$V_o = A_{v_{NL}} \frac{R_i}{R_i + R_s} V_s$$

$$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} A_{v_{NL}}}$$

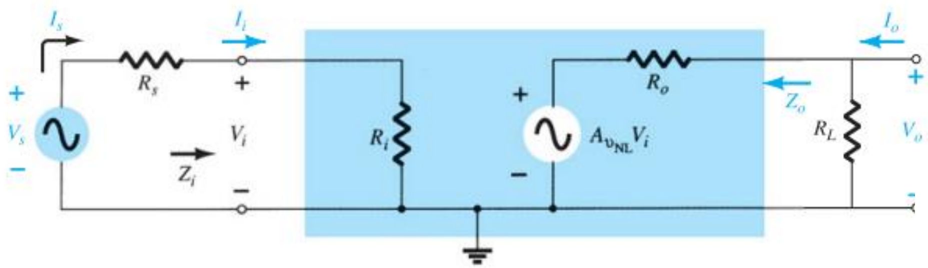


FIG. 5.65
Considering the effects of R_s and R_L on the gain of an amplifier.

$$\boxed{\frac{V_i}{V_s} = \frac{R_i}{R_i + R_s}}$$

$$V_o = \frac{R_L}{R_L + R_o} A_{v_{NL}} V_i$$

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L A_{v_{NL}}}{R_L + R_o} = \frac{R_L}{R_L + R_o} A_{v_{NL}}$$

$$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s}}$$

$$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{NL}}}$$

$$\boxed{A_{i_L} = -A_{v_L} \frac{R_i}{R_L}}$$

$$\boxed{A_{i_s} = -A_{v_s} \frac{R_s + R_i}{R_L}}$$

CASCADED SYSTEMS

Cascaded Systems

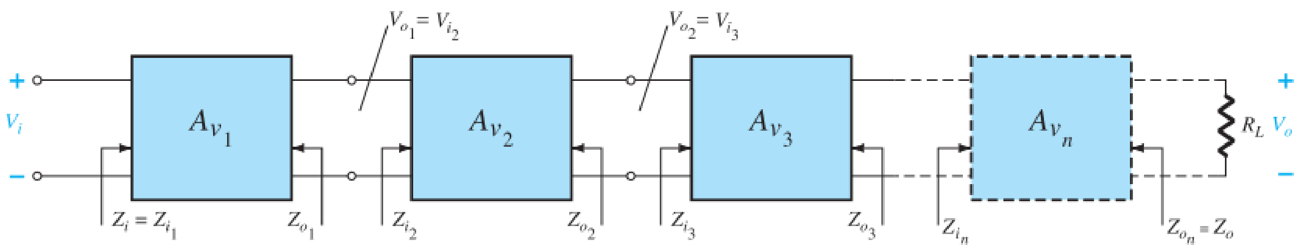
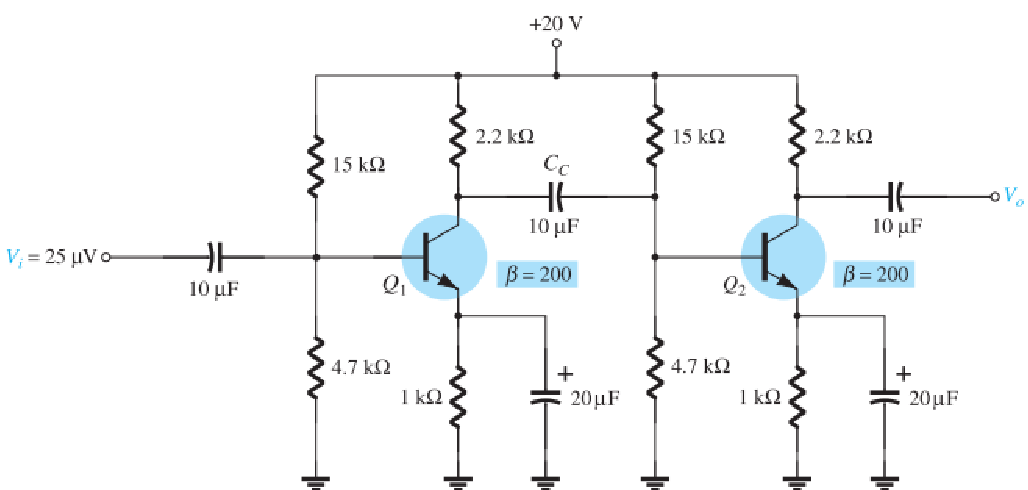


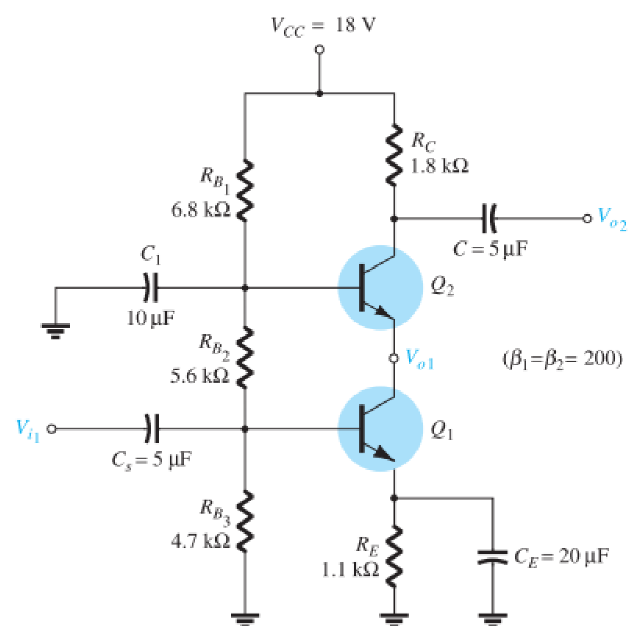
FIG. 5.67
Cascaded system.

$$A_{v_T} = A_{v_1} \cdot A_{v_2} \cdot A_{v_3} \cdots$$

$$A_{i_T} = -A_{v_T} \frac{Z_{i_1}}{R_L}$$

- Examples: RC Coupled ct & Cascode ct
- Check Examples: 5.15 & 5.16





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THE HYBRID EQUIVALENT MODEL

The Hybrid Equivalent Model

- The r_e model has the advantage that the parameters are defined by the actual operating conditions,
- the parameters of the hybrid equivalent circuit are defined in general terms for any operating conditions.

		Min.	Max.	
Input impedance ($I_C = 1$ mA dc, $V_{CE} = 10$ V dc, $f = 1$ kHz)	h_{ie}	0.5	7.5	kΩ
Voltage feedback ratio ($I_C = 1$ mA dc, $V_{CE} = 10$ V dc, $f = 1$ kHz)	h_{re}	0.1	8.0	$\times 10^{-4}$
Small-signal current gain ($I_C = 1$ mA dc, $V_{CE} = 10$ V dc, $f = 1$ kHz)	h_{fe}	20	250	—
Output admittance ($I_C = 1$ mA dc, $V_{CE} = 10$ V dc, $f = 1$ kHz)	h_{oe}	1.0	30	μS

FIG. 5.92
Hybrid parameters for the 2N4400 transistor.

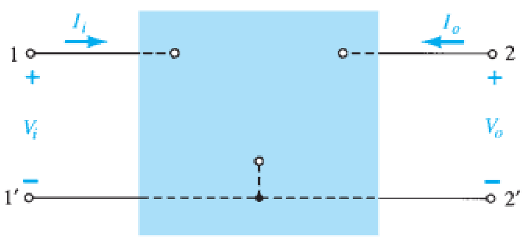


FIG. 5.93
Two-port system.

$$\boxed{V_i = h_{11}I_i + h_{12}V_o}$$

$$\boxed{I_o = h_{21}I_i + h_{22}V_o}$$

$$\boxed{h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0}}$$ ohms → short-circuit input-impedance parameter

$$\boxed{h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0}}$$ unitless → open-circuit reverse transfer voltage ratio parameter

$$\boxed{h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0}}$$ unitless → short-circuit forward transfer current ratio parameter

$$\boxed{h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0}}$$ siemens → short-circuit forward transfer current ratio parameter

Transistor Hybrid Equivalent ct

$$V_i = h_{11}I_i + h_{12}V_o$$

$$I_o = h_{21}I_i + h_{22}V_o$$

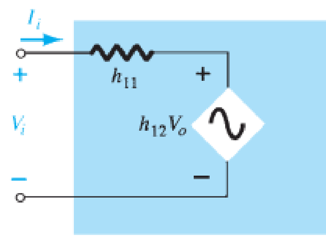


FIG. 5.94
Hybrid input equivalent circuit.

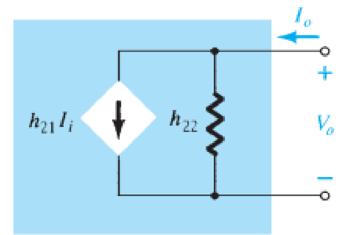


FIG. 5.95
Hybrid output equivalent circuit.

- For Transistor:

$h_{11} \rightarrow$ input resistance $\rightarrow h_i$
$h_{12} \rightarrow$ reverse transfer voltage ratio $\rightarrow h_r$
$h_{21} \rightarrow$ forward transfer current ratio $\rightarrow h_f$
$h_{22} \rightarrow$ output conductance $\rightarrow h_o$

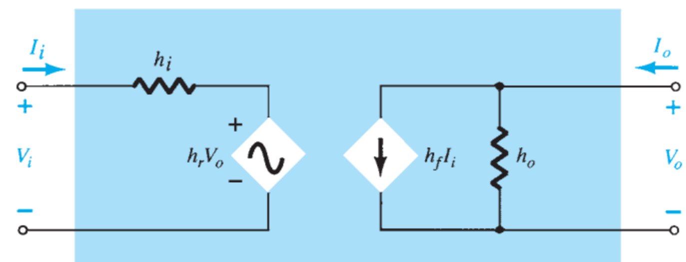


FIG. 5.96
Complete hybrid equivalent circuit.

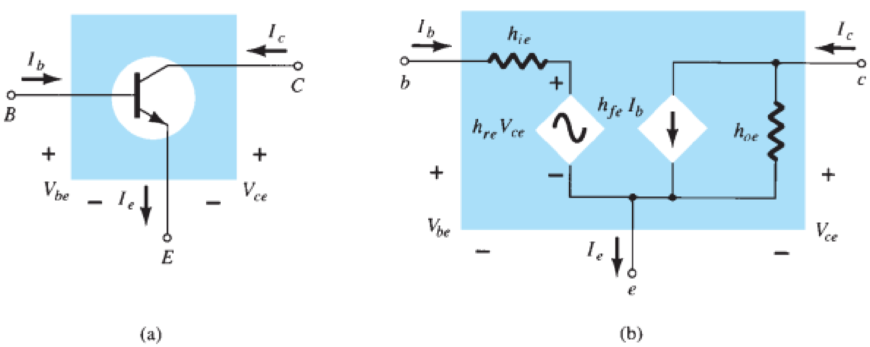


FIG. 5.97
Common-emitter configuration: (a) graphical symbol; (b) hybrid equivalent circuit.

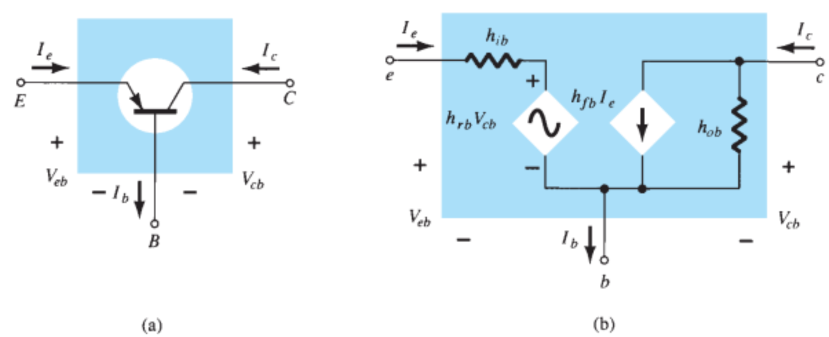


FIG. 5.98
Common-base configuration: (a) graphical symbol; (b) hybrid equivalent circuit.

Hybrid vs. r_e model

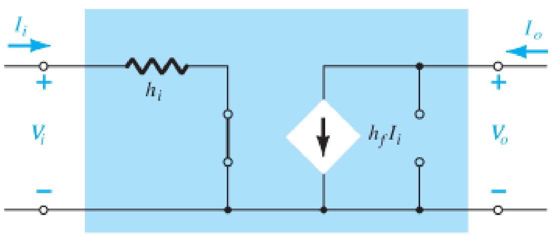


FIG. 5.99
Effect of removing h_{re} and h_{oe} from the hybird equivalent circuit.

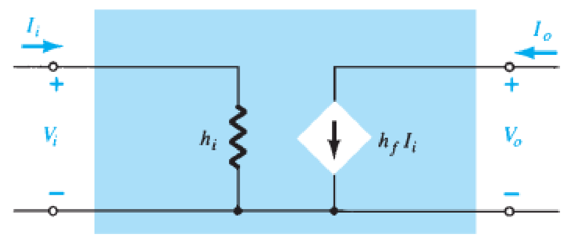


FIG. 5.100
Approximate hybrid equivalent model.

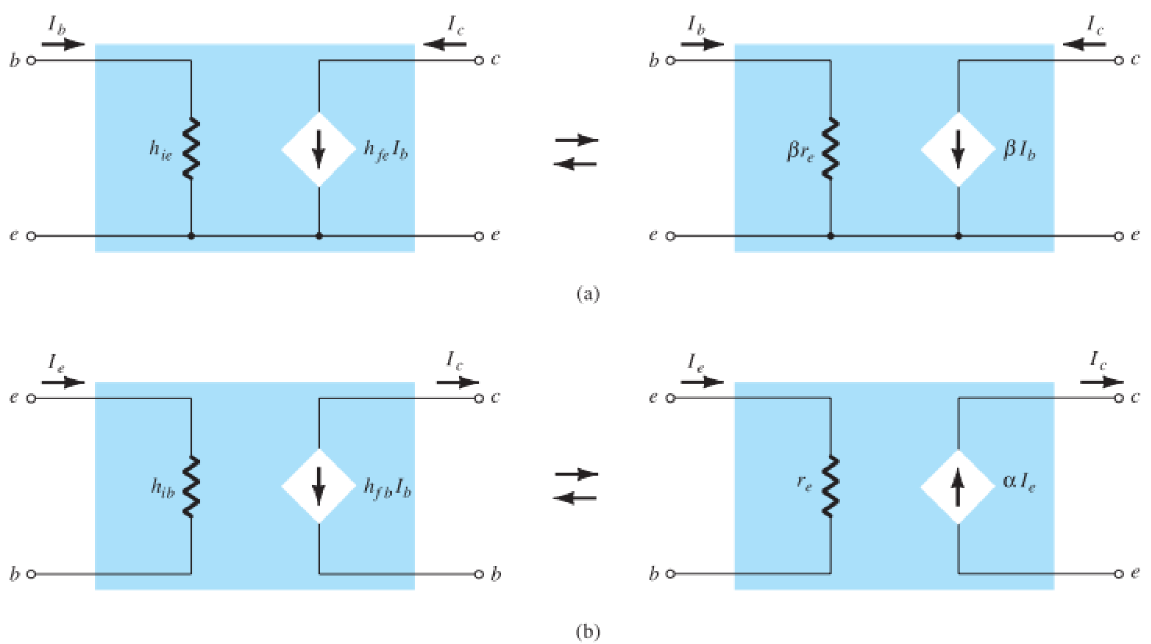


FIG. 5.101
Hybrid versus r_e model: (a) common-emitter configuration; (b) common-base configuration.

$\boxed{h_{ie} = \beta r_e}$

$\boxed{h_{fe} = \beta_{ac}}$

$\boxed{h_{ib} = r_e}$

$\boxed{h_{fb} = -\alpha \cong -1}$

APPROXIMATE & COMPLETE H-MODEL

Approximate h-model

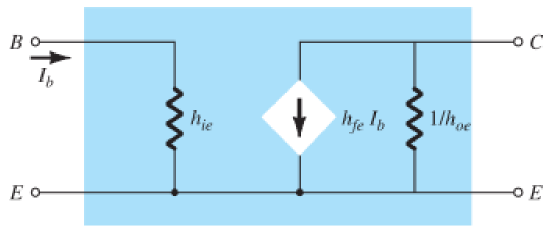


FIG. 5.104
Approximate common-emitter hybrid equivalent circuit.

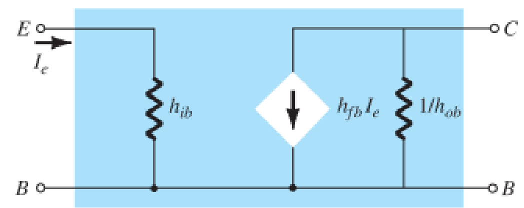


FIG. 5.105
Approximate common-base hybrid equivalent circuit.

- Fixed Bias ct

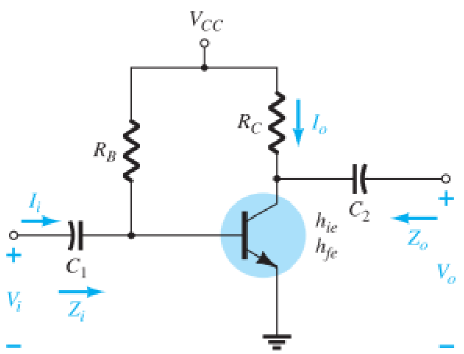


FIG. 5.106
Fixed-bias configuration.

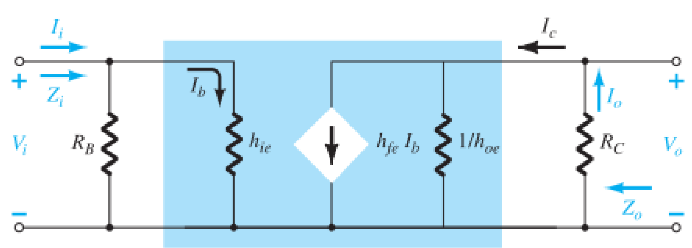


FIG. 5.107
Substituting the approximate hybrid equivalent circuit into the ac equivalent network of Fig. 5.106.

$$\boxed{Z_i = R_B \| h_{ie}}$$

$$\boxed{Z_o = R_C \| 1/h_{oe}}$$

$$R' = 1/h_{oe} \| R_C$$

$$V_o = -I_o R' = -I_C R' = -h_{fe} I_b R'$$

$$I_b = \frac{V_i}{h_{ie}}$$

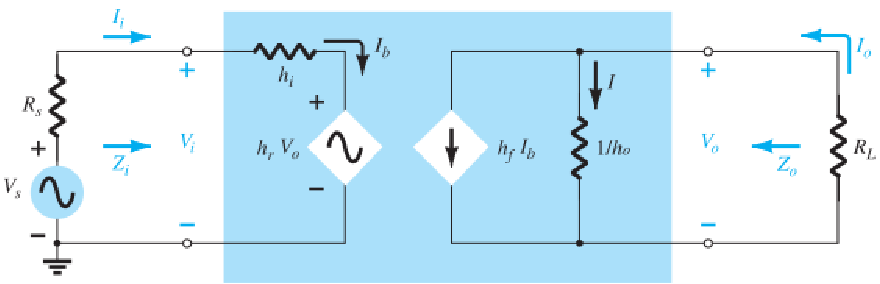
$$V_o = -h_{fe} \frac{V_i}{h_{ie}} R'$$

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{h_{ie}(R_C \| 1/h_{oe})}{h_{ie}}}$$

- Check other configurations !!

$$\boxed{A_i = \frac{I_o}{I_i} \cong h_{fe}}$$

Complete h-model



Current Gain, $A_i = I_o/I_i$

$$I_o = h_f I_b + I = h_f I_i + \frac{V_o}{1/h_o} = h_f I_i + h_o V_o$$

Substituting $V_o = -I_o R_L$ gives

$$I_o = h_f I_i - h_o R_L I_o$$

Rewriting the equation above, we have

$$I_o + h_o R_L I_o = h_f I_i$$

and $$I_o(1 + h_o R_L) = h_f I_i$$

so that $$\boxed{A_i = \frac{I_o}{I_i} = \frac{h_f}{1 + h_o R_L}}$$

Voltage Gain, $A_v = V_o/V_i$

$$V_i = I_i h_i + h_r V_o$$

$$I_i = (1 + h_o R_L) I_o / h_f$$

and $I_o = -V_o/R_L$

$$V_i = \frac{-(1 + h_o R_L) h_i}{h_f R_L} V_o + h_r V_o$$

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{-h_f R_L}{h_i + (h_i h_o - h_f h_r) R_L}}$$

Input Impedance, $Z_i = V_i/I_i$

$$V_i = h_i I_i + h_r V_o$$
$$V_o = -I_o R_L$$
$$V_i = h_i I_i - h_r R_L I_o$$
$$A_i = \frac{I_o}{I_i}$$

$$I_o = A_i I_i$$

$$V_i = h_i I_i - h_r R_L A_i I_i$$

$$Z_i = \frac{V_i}{I_i} = h_i - h_r R_L A_i \qquad A_i = \frac{h_f}{1 + h_o R_L}$$

$$\boxed{Z_i = \frac{V_i}{I_i} = h_i - \frac{h_f h_r R_L}{1 + h_o R_L}}$$

Output Impedance, $Z_o = V_o/I_o$

$$V_s = 0$$

$$I_i = -\frac{h_r V_o}{R_s + h_i}$$

$$I_o = h_f I_i + h_o V_o$$
$$= -\frac{h_f h_r V_o}{R_s + h_i} + h_o V_o$$

$$\boxed{Z_o = \frac{V_o}{I_o} = \frac{1}{h_o - [h_f h_r/(h_i + R_s)]}}$$

HYBRID Π MODEL

Hybrid π Model

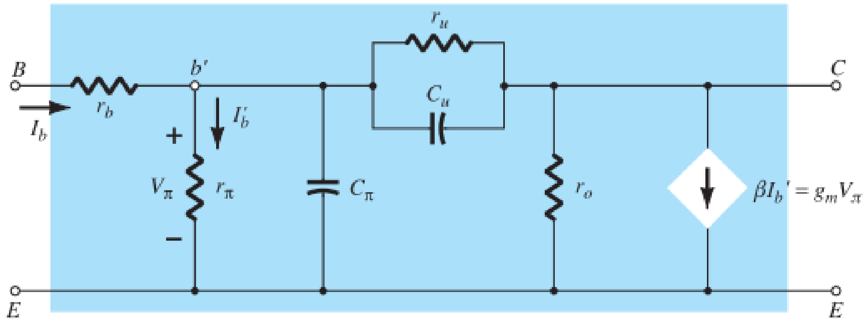


FIG. 5.123
Giacoletto (or hybrid π) high-frequency transistor small-signal ac equivalent circuit.

$$\boxed{r_\pi = \beta r_e}$$

$$\boxed{r_o = \frac{1}{h_{oe}}}$$

$$\boxed{g_m = \frac{1}{r_e}}$$

$$\boxed{\frac{r_\pi}{r_\pi + r_u} \cong \frac{r_\pi}{r_u} \cong h_{re}}$$

VARIATIONS OF TRANSISTOR PARAMETERS

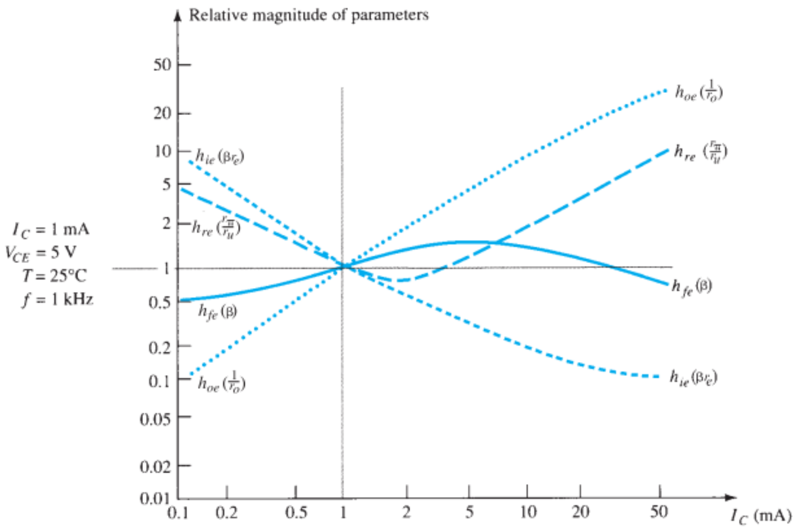


FIG. 5.124
Hybrid parameter variations with collector current.

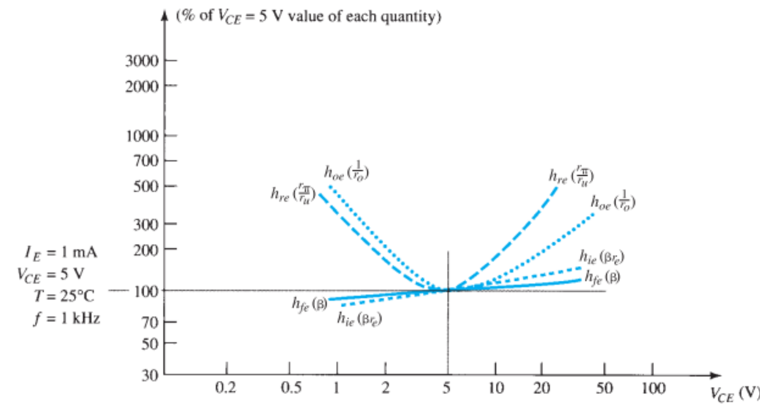


FIG. 5.125
Hybrid parameter variations with collector–emitter potential.

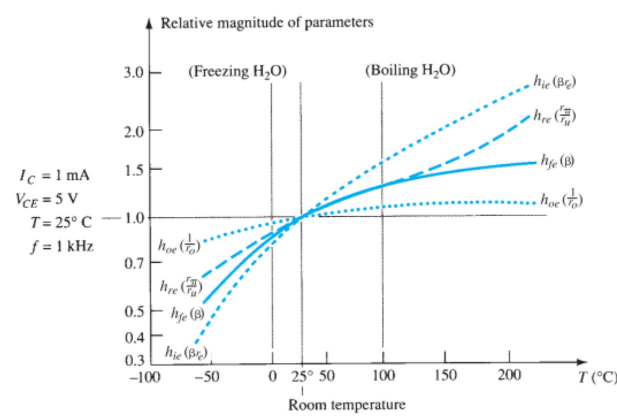


FIG. 5.126
Hybrid parameter variations with temperature.

TROUBLESHOOTING & PRACTICAL APPLICATIONS

Troubleshooting

In general, therefore, if a system is not working properly, first disconnect the ac source and check the dc biasing levels.

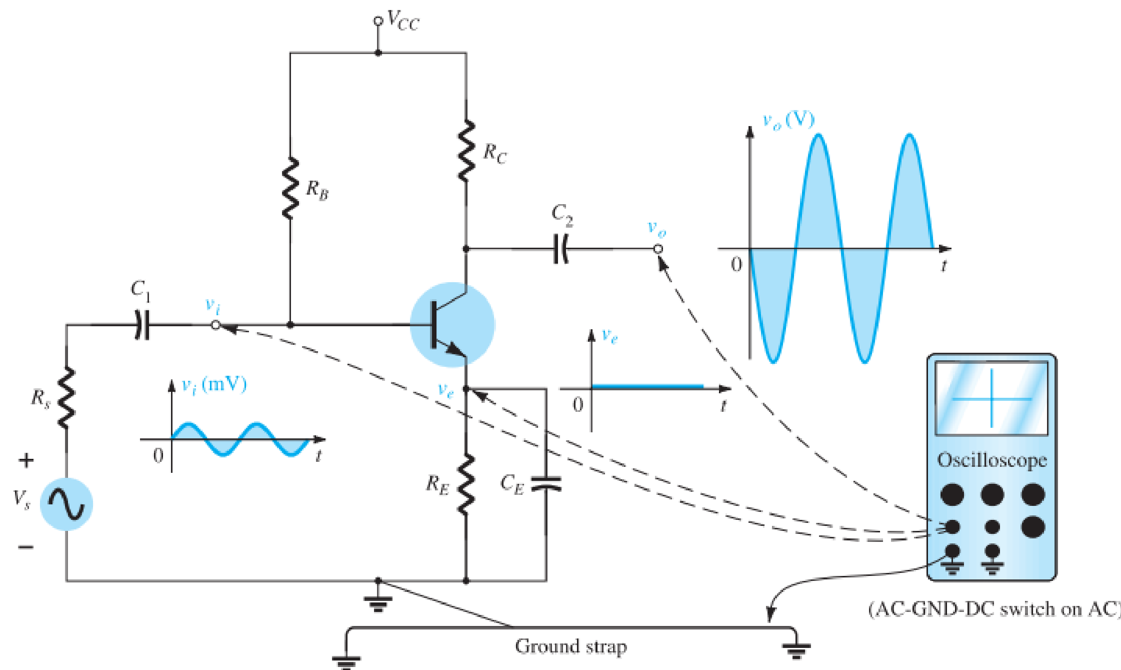


FIG. 5.128
Using the oscilloscope to measure and display various voltages of a BJT amplifier.

PRACTICAL APPLICATIONS

- Audio Mixer

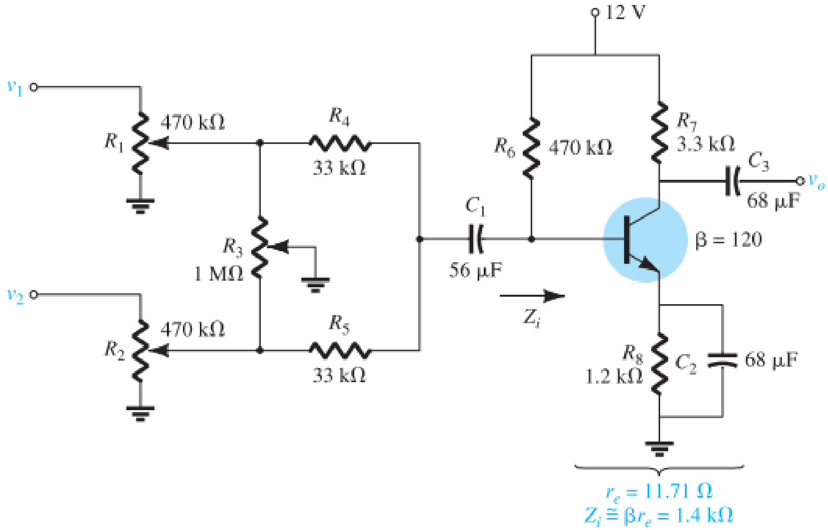


FIG. 5.130
Audio mixer.

- Preamplifier

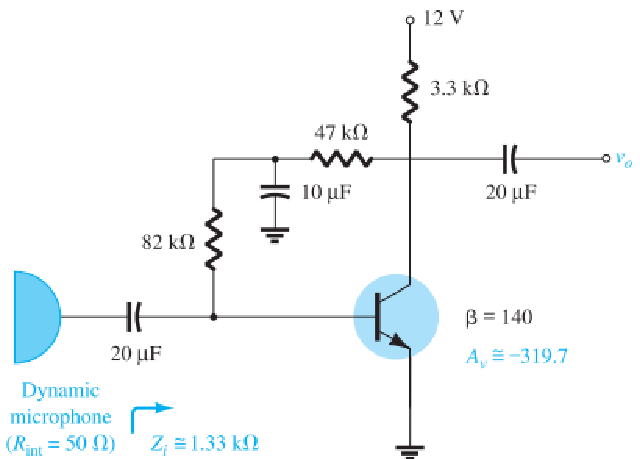


FIG. 5.133
Preamplifier for a dynamic microphone.

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- For more details, refer to:
  - Chapter 5, Electronic Devices and Circuits, Boylestad.
- The lecture is available online at:
  - https://speakerdeck.com/ahmad_elbanna
- For inquires, send to:
  - ahmad.elbanna@feng.bu.edu.eg